formed in such border areas. In other respects the wafer and its treatment and further processing is the same as that described for the wafer of FIG. **1**. For this version of the master slice, the wafer form presented in FIG. **15***a* may be used. FIG. **15***a* partially illustrates the wafer at the same stage of processing existing as the wafer of FIG. **5***c*, earlier discussed in connection with the preceeding embodiments.

On a custom essentially hand made basis, wafers may be fabricated to the designs discussed in connection with the embodiment of FIG. **1**. However, it has been found that inherent deficiencies in production semiconductor processing to date does not provide adequate processing in the peripheral border areas of the wafers employed in this invention. Transistors formed in those peripheral areas more often than not do not meet the high standards required and are, hence, regarded as defective. The reasons why present production processing is so limited is not known to applicants. As a practical matter thus it is thought preferable simply to eliminate formation of transistors in those border areas, thereby avoiding any temptation of the designer to use that unavailable geography; hence, the version of the invention presented in FIGS. **14** and **15***a* in this description results. In a sense this form of the invention reduces the scope of space utilization efficiency that may be achieved at least in mass production as less transistors are formed and, hence, in that sense the structure is less preferred. Nontheless the use of the total area of the wafer to achieve the greatest population of transistors, as in the embodiment of FIG. **1**, remains as a goal, and is dependent upon future improvement in chemical processing production technology.

Additionally since most dies or chips formed on the wafer are formed of transistors arranged in a rectangular shape pattern, as is the custom in the industry, there will also be some additional wafer geography that is not used. This results from fitting those rectangular shaped areas within the wafer's central region with the outermost corner of the rectangle being located near or even touching the inner edge of the border strip, which as shown is generally circularly curved. Consequently with two adjacent rectangular areas formed with transistors and with those adjacent rectangular areas slightly horizontally displaced from one another, as example, referring again to FIG. **14**, an additional generally triangular area of the wafer, is formed between the sides and corners of such adjacent rectangular areas, such as chips **352** and **354** and curved border strip **350**, such as illustrated at **356**, **358**, and the border strip in FIG. **14**. Forming transistors in those triangular areas or not is regarded as a designer's choice. From a broader perspective the outer edges of the rectanguar shape of the formed semiconductor chips together create a stair case appearance as shown. Looking at the border area in that case, the inner edge of the border area defines a stair case appearance and is not simply a web like band. Although satisfactory transistors may be formed in such triangular area, one might choose not to do so, since those transistors would not be used as part of any die or chip being formed on the wafer. Should one decide to eliminate formation of transistors in those areas, the underlying wafer, at the stage of processing corresponding to that earlier discussed in connection with FIG. **5***c*, would appear as in FIG. **15***b*.

The alternative embodiment for the wafer illustrated in FIG. **16** incorporates not only the principle of a void peripheral border area **350** that was earlier described in connection with FIGS. **14** and **15***a* but also uses the void or island within the more central regions of the wafer in which to position the alignment markers as was earlier described and used in connection with the emboidiment of FIG. **13**. As the reasons have been adequately separately discussed in connection with the prior figures, they are not here repeated.

The expanse of the sea formed by the standard gates covers a great enough region of the wafer to include therewithin many rectangular shaped areas, at least two, in which semiconductor chips are to be formed. Within each of those rectangular shaped areas the gates are capable of being formed into an input circuit and at least some portion of the gates are ultimately used for that purpose. Similarly within each of those rectangular shaped areas the gates are also capable of being formed into an output circuit and at least some portion of the gates are ultimately used for that purpose. Gates not used for either of the preceeding purposes, typically the majority of gates within each rectangular region is used for other circuit purposes. The foregoing generalization is applicable irrespective of whether or not any one or more of such rectangular shaped regions subsumes or includes the islands, described earlier.

It is believed that the foregoing description of the preferred embodiments of the invention are sufficient in detail to enable one skilled in the art to make and use the invention. However, it is expressly understood that the details of the elements which are presented for the foregoing enabling purpose is not intended to limit the scope of the invention, in as much as equivalents to those elements and other modifications thereof, all of which come within the scope of the invention, become apparent to those skilled in the art upon reading this specification. Thus the invention is to be broadly construed within the full scope of the appended claims.

What is claimed is:

1. A master slice, comprising:

a semiconductor wafer;

a sea of gates formed in and covering substantially the entire surface of said semiconductor wafer, said sea of gates defining a configurable gate array having a continuum of transistors from which at least one application specific integrated circuit (ASIC) chip is capable of being formed by selectively connecting together a subset of the continuum of transistors and cutting through unconnected transistors to separate the ASIC chip from the wafer, said configurable gate array being free of predefined boundaries along which the semiconductor wafer must be cut; and

a plurality of islands in said sea of gates and separate from the transistor continuum for aiding in forming the ASIC chip prior to its separation from the wafer.

2. The master slice as defined in claim **1** wherein at least one of said plurality of islands contains an alignment marker.

3. The master slice as defined in claim **2** wherein at least one of said plurality of islands contains test means for evaluating characteristics of said master slice.

4. The master slice as defined in claim **3** wherein at least one of said plurality of islands contains an application specific integrated circuit.

5. The master slice as defined in claim **1** wherein said sea of gates are arranged in rows and columns.

6. The master slice as defined in claim **5** wherein at least one of said plurality of islands comprises an alignment marker; and wherein at least one other one of said plurality of islands comprises a non-gate array semi-custom circuit, including semiconductor devices of types different from said at least one transistor forming said sea of gates.

7. A master slice, comprising:

a semiconductor wafer;

said semiconductor wafer having a surface of predeter-